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C-V ANALYSIS AT VARIABLE FREQUENCY OF MOS STRUCTURES WITH DIFFERENT GATES, CONTAINING Hf-DOPED TA_2O_5

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Abstract. The quality of the interface between the insulating layer and the Si substrate in contemporary submicron MOS technology is a critical issue for device functioning. It is characterized through the electrically active defect centers, known as interface states. Their response to the frequency is discussed here, by analyzing capacitance-voltage and conductance-voltage curves. The *C-V* method is preferred in many cases, since it offers easy measurement, and it is applied to extract information about interface traps and fixed oxide charge, at different frequencies. This technique, related with frequency dependent *G-V* measurements, can be very useful in characterizing charge trapped in the dielectric and at the interface with Si. By extracting the value of frequency dependent flatband voltage, we have obtained the fixed oxide charges at flatband condition. A comparison between the results obtained by two different methods is made. The samples that are studied are metal-insulator-semiconductor (MIS) structures that include high-*k* dielectric as insulating layer (Hf doped Ta_2O_5), with thickness of 8 nm, with different metal used as gate electrode. Here the influence of the top electrode on the generation and behavior of the traps in the oxide layer is discussed. The results show that the value of metal work function of the gate material is an issue that should be considered very carefully, especially in the case of high work function metal gates, when generation of extra positive charge than in the case of other metals is observed.

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1. INTRODUCTION

The introduction of high-*k* materials as a replacement of SiO_2 in various microelectronic applications requires profound knowledge of the properties of high-*k* dielectric materials, especially the properties related with certain applications, for which high-*k* candidates have proved themselves as most suitable dielectrics. Among them Ta and Hf oxides meet the requirements for application in dynamic random access memories (DRAM's) and MOSFET's, respectively [1,2]. Pure Ta_2O_5, with its high storage ability (i.e. high permittivity in combination

with high breakdown field) and low leakage current is studied in detail. The main drawbacks of Ta_2O_5, identified as its thermodynamic instability on contact with Si, which leads to the formation of lower-*k* interfacial layer and its relatively small bandgap (4–4.5 eV), which defines small barrier heights for carrier injection, hence increased leakage current, are tailored by doping of Ta_2O_5 with a proper element or by mixing it with another oxide. It is shown [3] that this approach indeed could extend the potential of pure Ta_2O_5 as a high-*k* material, because the process of mixing HfO_2 and Ta_2O_5 modifies the dominant conducting mechanisms and changes the traps parameters as compared with pure Ta_2O_5 stacks with the same high-*k* dielectric thickness.

The aspect of the influence of top metal electrode on electric parameters of the devices with high-*k* material [4–6], especially on the evolution of degradation mechanisms and generation and behavior of bulk and interfacial traps, uncovers a lot of unsolved problems that require further studying. This especially refers to the metals with higher value of work function when used as gate electrodes on doped high-*k* structures.

2. EXPERIMENTAL

Chemically cleaned p-type (100) Si wafers with resistivity of 15 Ωcm were used as substrates. Tantalum oxide was deposited by reactive sputtering of a Ta target in an Ar + 10% O_2 atmosphere obtaining Ta_2O_5 layer approximately 7.5 nm thick; the working gas pressure was 0.33 Pa and rf power density was 3.6 W/cm^2. The Si substrate was heated at 200 °C during deposition. The Hf-doped Ta_2O_5 layers were obtained by deposition of Hf layer ~ 0.7 nm thick on the top of previously deposited Ta_2O_5 layer. Hf was deposited by sputtering of a Hf target in an Ar atmosphere. The samples were subjected to a post-deposition annealing at 400°C in N_2 for 30 min in order to mix the two layers and to ensure the diffusion of Hf into the matrix of Ta_2O_5, resulting in an 8 nm thick final layer. Top electrodes of MOS structures were formed by sputtering of TiN, Mo, Pt and Ta in an Ar atmosphere. Fabrication sequence ended with post metallization annealing in forming gas at 450 °C for 1 h.

The samples were studied by means of *C-V* measurements, at different frequencies 50 kHz, 100 kHz, 200 kHz, 500 kHz and 1 MHz, which means that the structures are tested both under low and high frequency conditions. From these measurements frequency dependence of the value of flatband voltage and fixed oxide charges is observed. For determining these values, also, the *G-V* method was used. The results obtained by these two different methods are compared.

3. RESULTS AND DISCUSION

When a MOS structure is in the depletion region, applying small ac signal causes oscillations of the Fermi level around the mean position governed by the dc bias. In these conditions the presence of interfacial states and their response to the measurement, changes the value of measured capacitance. It can be seen from the Fig. 1 that at low frequencies, the values

of capacitance of all studied structures that contain different metal gates, are higher than at high frequencies. The higher values of capacitance at low frequencies are due to excess capacitance resulting from the interface states in equilibrium with the Si-substrate that can follow the ac signal. This observation has been attributed to the capacitive response of interface states to the measurement in the case of silicon dioxide insulating layers [7] and also was observed in the case of Ta_2O_5 thin films [8]. At high frequencies the charges at the interface states cannot follow an ac signal, making no (or negligibly small) contribution of interface capacitance to the total capacitance. In the case of stacked high-*k*/ SiO_2 dielectric layers, the contribution of the border traps to the capacitance, also, has to be taken into account [9]. Since we study Ta_2O_5:Hf/SiO_2 dielectrics, it is expected that the contribution of the border traps in the Ta_2O_5:Hf layer, will be significant, which is confirmed by the measurement.

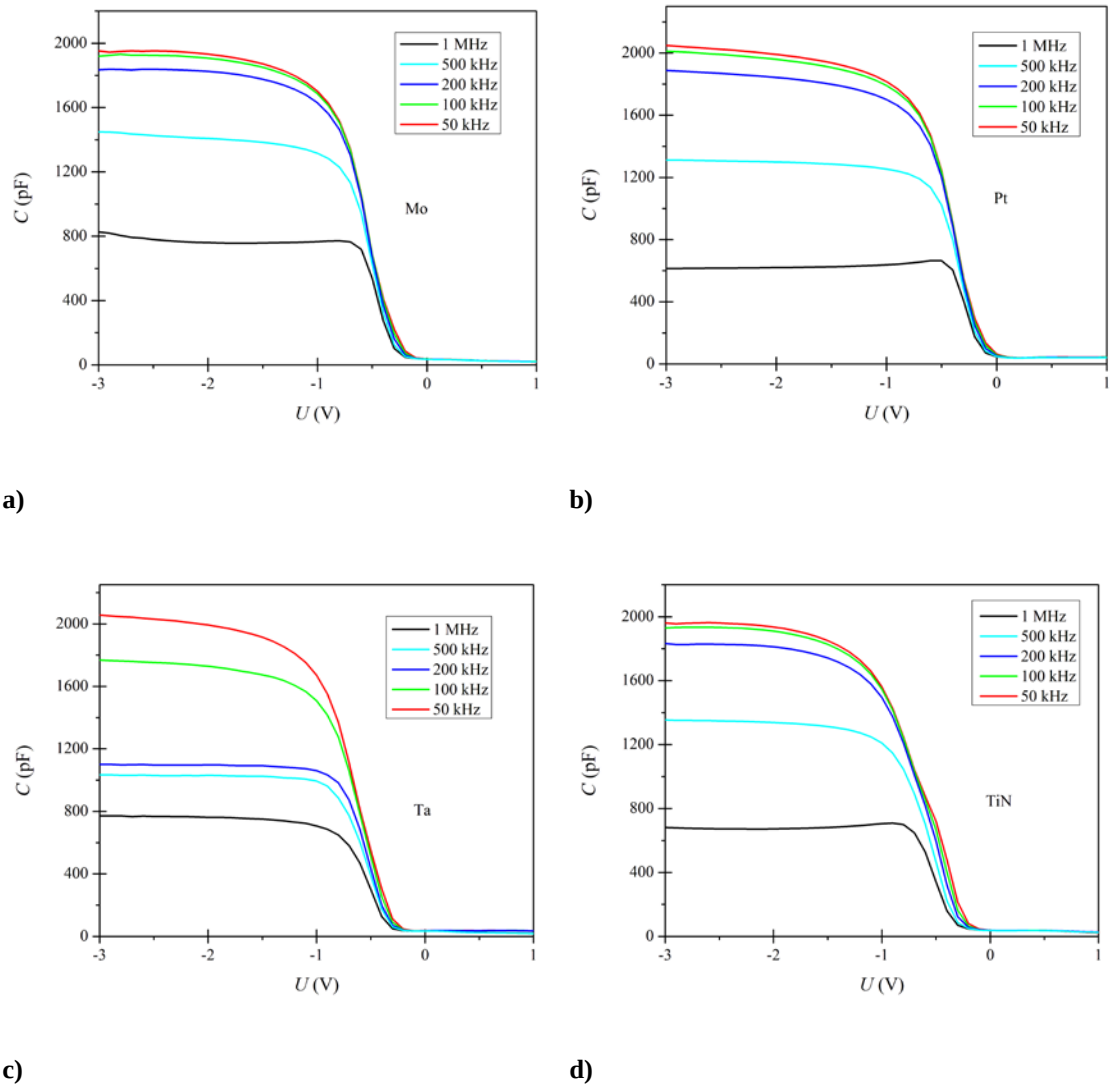

Fig. 1: Frequency dispersion of *C-V* curves of Ta_2O_5:Hf/SiO_2/Si structure, with a) Mo; b) Pt; c) Ta and d) TiN as top electrode. The capacitance alteration is measured in both directions, i.e. this represents the hysteresis of *C-V* curves.

For all samples from the obtained *C-V* curves, lowest values of capacitance in accumulation at the highest frequencies (1 MHz) were obtained (Fig.1). This observation is the same as in the case of pure Ta_2O_5, Hf doped Ta_2O_5 with Al gate and also it is observed here, in the case of Hf doped Ta_2O_5 samples with different gate electrodes (Mo, Pt, Ta and TiN). The observed hysteresis was negligible, leading to very low slow states density of the order of 10^{10} cm^{-2}.

From *C-V* curves and using the method of extraction of the values of capacitance in accumulation [10], we have obtained the values of flatband voltage and fixed oxide charges, using the standard capacitance method [11,12]. Flatband voltage is the voltage corresponding to the value of flatband capacitance (C_{FB}), calculated according to the equation (1):

$$C_{FB} = \frac{\frac{C_{acc}\varepsilon_s A}{\lambda}}{C_{acc} + \frac{\varepsilon_s A}{\lambda}}, \tag{1}$$

where C_{acc} is the capacitance in accumulation, ε_s is the permittivity of the substrate material (Si), A is the gate area and λ is the extrinsic Debye length, as calculated by:

$$\lambda = \sqrt{\frac{\varepsilon_s kT}{q^2 N_a}}, \tag{2}$$

where kT is the thermal energy at room temperature, q is the electron charge and N_a is the acceptor concentration in silicon. If the value of N_a is not given by the manufacturer of the substrate, it can be calculated by plotting the voltage dependence of $1/C^2$ [11, 12], given by the following expression

$$\frac{\partial\left(1/C^2\right)}{\partial U} = \frac{2}{q\varepsilon_0\varepsilon_s N_a A^2}. \tag{3}$$

The acceptor concentration is calculated from the slope of this plot, as presented at Fig. 2. Once the value of C_{FB} is known, the value of V_{FB} can be obtained from the *C-V* curve data, by interpolating between the closest gate-to-substrate voltage values.

Fixed oxide charges Q_{ox} for samples with different metal gates were determined, using the equation

$$V_{FB} - W_{MS} = -\frac{Q_{ox}}{C_{acc}}, \tag{4}$$

where V_{FB} is the flatband voltage, W_{MS} is the metal-semiconductor work function, and C_{acc} is the oxide capacitance. The values of metal work functions for Mo, TiN, Pt and Ta taken from literature are as follows, 4.2 eV, 4.7 eV, 5.6 eV and 4.25 eV, respectively. The obtained surface densities of the fixed charges, for samples with various gates, calculated using flatband voltage values obtained by *C-V* curves, are presented in Table 1.

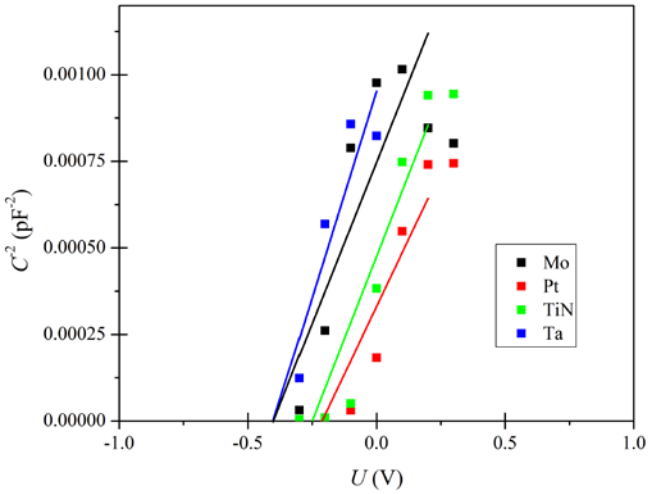

Fig. 2: Extraction of the acceptor concentration N_a of the substrate from *C-V* curves of Ta_2O_5:Hf/SiO_2/Si structure, with Mo, Pt, Ta and TiN as top electrode.

The presence of the interface states is evident also by their influence on the measured conductance at different frequencies (Fig. 3). Here, same as in the case of frequency dependence of *C-V* curves, there isn't any dependence of the metal used as a gate, because the frequency dependence of capacitance, as well as of conductance is due to the interfacial charges, present at the interface of the insulating layer (in this case doped Ta_2O_5 and intermediate SiO_2) and the Si substrate. The quality of this interface is the same for all samples, since they belong to the same manufacturing sequence, and only differ in the deposited top metal gate. G/ω-*V* curves give a pick, which is positioned at the flatband voltage. Such behavior of the G/ω peaks is attributed to particular distribution of surface states between Si/oxide interface [13]. Using this fact, we will extract the values of flatband voltage also from G/ω-*V* curves, in order to make a comparison between these two methods. These values are also presented in Table 1.

From the values presented in Table 1, it can be seen that both methods give very similar values of flatband voltage. These values show tendency to increase with the rise of the measuring frequency. This shift of flatband voltage toward higher values is due to the response of interfacial states at the interface oxide/Si substrate, that at lower frequencies contribute in the overall capacitance of the structure, which is not the case at higher frequencies. Here the influence of the gate electrode becomes obvious, since it is also included in the definition of the value of flatband voltage by equation (4). Flatband voltage for samples with Mo, Ta and TiN gate (which have similar values metal work function) are close to each other, while in the case of Pt (gate with highest work function) different values of flatband voltage are obtained.

Also it can be seen that the calculated values of oxide charges for Mo, Ta and TiN are similar, while for Pt gate it is substantially higher, i.e. in these samples an extra positive charge exists. This observation is related with the nature of the interface at the contact between the oxide and the gate. In the case of high work function metal, the position of metal Fermi level favors the transition of electrons from the oxide layer into metal conduction band, thus leaving uncompensated positive charge in the interfacial region. The presence of this extra positive

charge is registered in our calculations, too, whose values as presented in Table 1 are almost one order of magnitude higher than in the case of other gates, which are not labeled as high work function metals.

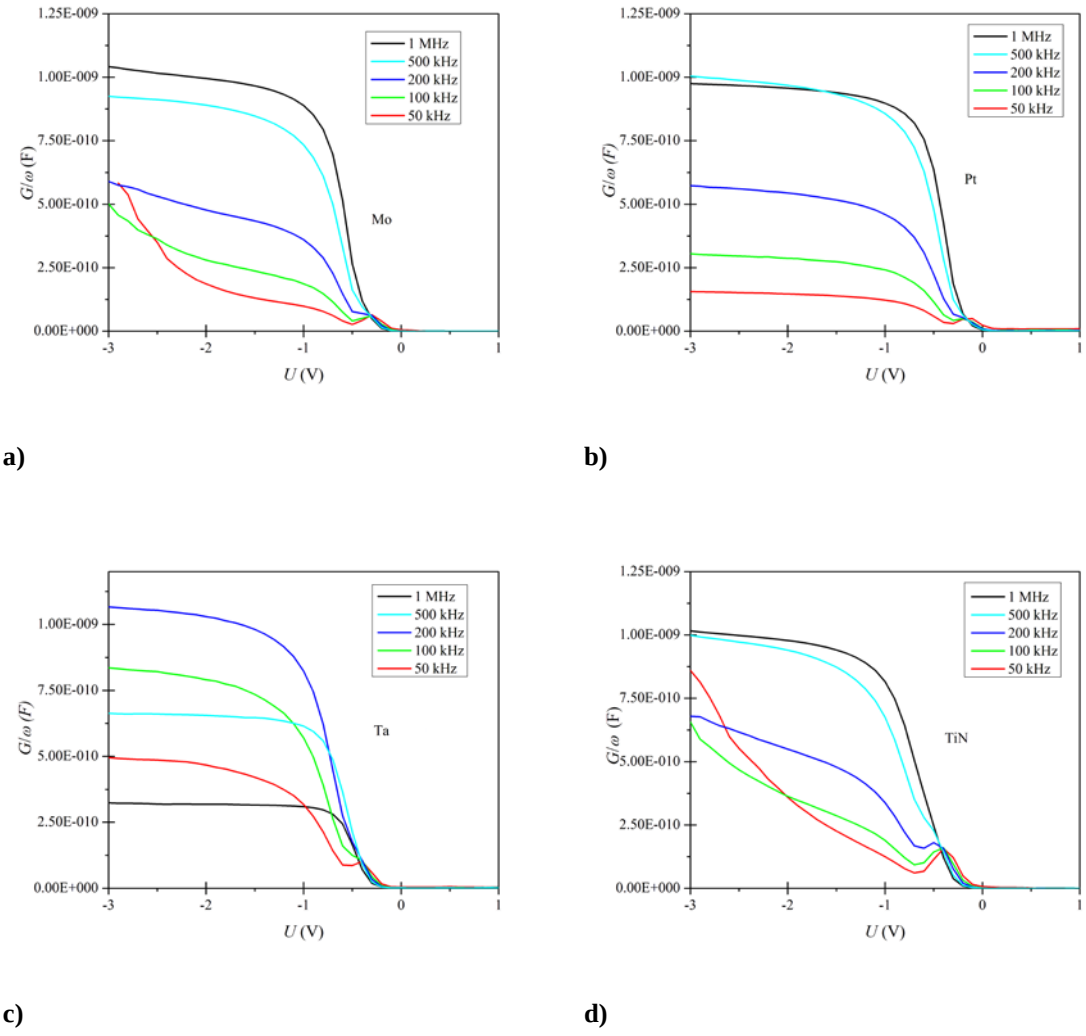

Fig. 3: Frequency dispersion of G/ω-V curves of Ta_2O_5:Hf/SiO_2/Si structure, with a) Mo; b) Pt; c) Ta and d) TiN as top electrode. The pick position corresponds to the value of flatband voltage

Table 1 Extracted values of flatband voltage and fixed oxide charges from two different methods, from C-V curves and from the peack position of G/ω-V curves

f (kHz)	C_{acc}(pF)	C_{fb}(pF) (C-U)	U_{fb} (V) (C-U)	Q_{ox} (C/cm^2)·10^{11}	U_{fb} (V) (G-U)	C_{acc}(pF)	C_{fb}(pF) (C-U)	U_{fb} (V) (C-U)	Q_{ox} (C/cm^2)·10^{11}	U_{fb} (V) (G-U)
	TiN					**Ta**				
50	1960	286	**0.32**	5.88	**0.38**	2050	288	**0.4**	10.3	**0.4**
100	1929	286	**0.35**	7.23	**0.42**	1760	282	**0.41**	9.24	**0.44**
200	1826	283	**0.38**	8.22	**0.49**	1100	257	**0.43**	6.33	**0.49**
500	1353	269	**0.42**	7.44	**0.52**	1030	253	**0.44**	6.18	**0.5**

1000	680	225	**0.43**	3.91	**0.57**	770	234	**0.47**	5.2	**0.53**
	Mo					**Pt**				
50	1950	286	**0.33**	6.34	**0.28**	2040	288	**0.19**	45.9	**0.12**
100	1920	286	**0.34**	6.72	**0.3**	2000	287	**0.2**	45.5	**0.15**
200	1840	284	**0.36**	7.36	**0.32**	1890	285	**0.21**	43.5	**0.18**
500	1450	272	**0.37**	6.16	**0.45**	1310	267	**0.21**	30.1	**0.24**
1000	827	239	**0.38**	3.72	**0.48**	620	218	**0.22**	14.4	**0.27**

The extracted values of flatband voltage by two methods and their frequency dependence are shown on Fig. 4. Fig. 5 presents frequency dependence of calculated oxide charges, for samples with different gates. It can easily be seen that only in the case of Pt gate, frequency dispersion is observed.

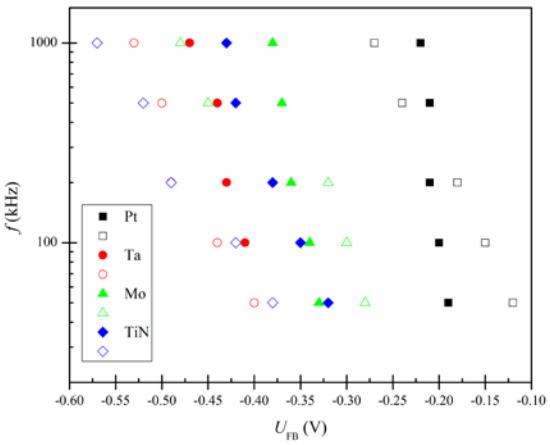

Fig. 4: Frequency dispersion of extracted values of flatband voltage for samples with different gates. Solid symbols are presenting the values obtained from *C-V* curve and open ones are for the values obtained by *G-V* curves.

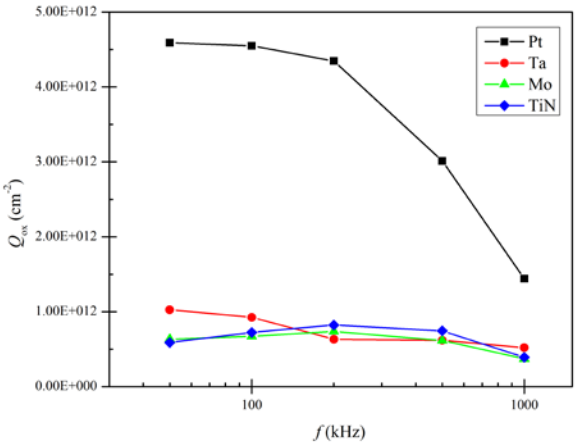

Fig. 5: Frequency dispersion of calculated surface density of fixed oxide charges, for samples with different gates.

4. CONCLUSION

In this paper we have characterized samples that contain Hf doped Ta_2O_5, alternative dielectric, marked as high-*k* material. Here we analyze the quality of the interfaces of this multilayered structure, the interface between oxide/Si substrate and metal/oxide interface. The presence of interfacial electrically active states is confirmed by their response to the measuring frequency, and therefore their influence to the flatband voltage. These values are calculated using both *C-V* and G/ω-*V* measurements, which converges toward similar values. The influence of the metal gate is strongest in the case of high work function metal, which leads to the creation of extra positive charges. These positive states are responsible for other phenomena, like charge trapping observed in the case of high work function metal gate, which is out of the scope of this paper.

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